IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

COPY

Applicant: Brett L. Williams

Title: SYSTEM SUPPORTING MULTIPLE MEMORY MODES INCLUDING A BURST EXTENDED DATA OUT MODE

Docket No.: 303.164US3
Filed: February 22, 2000
Examiner: Hong Kim

Serial No.: 09/510,375
Due Date: N/A
Group Art Unit: 2185

Commissioner for Patents
Washington, D.C. 20231

We are transmitting herewith the following attached items (as indicated with an "X"):

X A return postcard.
X Supplemental Preliminary Amendment (6 Pages).
X A Supplemental Information Disclosure Statement (1 pgs.), Form 1449 (1 pgs.), and copies of 4 cited references.
X A check in the amount of $180.00 to cover the fee for consideration of Information Disclosure Statement under 97(c).
X A check in the amount of $552.00 to cover the fee for additional claims as calculated below.

If an additional fee is required due to changes to the claims, the fee has been calculated as follows:

CLAIMS AS AMENDED						
	(1) Claims Remaining After Amendment		(2) Highest Number Previously Paid For	(3) Present Extra	Rate	Fee
TOTAL CLAIMS	24	-	20	4	x 18 =	$72.00
INDEPENDENT CLAIMS	16	-	10	6	x 80 =	$480.00
[ ] MULTIPLE DEPENDENT CLAIMS PRESENTED						$0.00
TOTAL						$552.00

Please consider this a PETITION FOR EXTENSION OF TIME for sufficient number of months to enter these papers and please charge any additional required fees or credit overpayment to Deposit Account No. 19-0743.

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)

By: Edward J. Brooks, III
Atty: Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, Washington, D.C. 20231, on this 19th day of September, 2001.

Amy Moriarty
Name

Amy Moriarty
Signature

Customer Number 21186
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. Box 2938, Minneapolis, MN 55402 (612-373-6900)
(GENERAL)

APPENDIX A

Copy of Supplemental Preliminary Amendment filed on September 19, 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Brett L. Williams	Examiner: Hong Kim
Serial No.:	09/510,375	Group Art Unit: 2185
Filed:	February 22, 2000	Docket: 303.164US3
Title:	SYSTEM SUPPORTING MULTIPLE MEMORY MODES INCLUDING A BURST EXTENDED DATA OUT MODE	

SUPPLEMENTAL PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

When the above-identified application is taken up for consideration, please amend the application as follows:

IN THE CLAIMS

Please add the following new claims 40-49:

40. (New) A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

41. (New) The system of claim 40, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

42. (New) A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller, wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

43. (New) A system, comprising:

a processor;

a memory controller coupled to the processor; and

a memory coupled to the memory controller, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second modes.

44. (New) The system of claim 43, wherein the power up detection circuit is responsive to a signal from the power supply to program the memory controller in accordance with the first and second modes.

45. (New) A system, comprising:

a processor;

a memory controller coupled to the processor; and

a memory coupled to the memory controller, wherein the memory includes a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory,

further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements.

46. (New) The system of claim 45, wherein the power up detection circuit is responsive to a signal from the power supply to program the memory controller in accordance with the first and second sets of requirements.

47. (New) A system, comprising:

a processor;

a memory controller coupled to the processor; and

a memory coupled to the memory controller, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank, the access control signals being driven in the first and second modes in response to information obtained by reading the first and second banks, respectively;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power

up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second modes.

48. (New) The system of claim 47, wherein the power up detection circuit is responsive to a signal from the power supply to program the memory controller in accordance with the first and second modes.

49. (New) A system, comprising:

a processor;

a memory controller coupled to the processor; and

a memory coupled to the memory controller, wherein the memory includes a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory, and controls access of the first bank in accordance with one of the first and second sets of requirements based on information obtained by reading the first bank, and controls access of the second bank in accordance with one of the first and second sets of requirements based on information obtained by reading the second bank;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements and to program the memory controller in accordance with the first and second sets of requirements.

REMARKS

Currently claims 26-49 are pending in this application. The Examiner is invited to contact the below-signed attorney to discuss any questions which may remain with respect to the present application.

Respectfully submitted,

BRETT L. WILLIAMS

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6913

Date 9/19/2001 By _____
Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 19th day of September, 2001.

Amy Moriarty
Name

Amy Moriarty
Signature

Docket No. 303.164US3
WD # 351492

Micron Ref. No. 94-0122.19

Clean Version of Pending Claims

APPARATUS HAVING MULTIPLE MEMORY MODES
Applicant: Brett L. Williams
Serial No.: 09/510,375

Claims 26-49, as of September 19, 2001 (date of supplemental preliminary amendment).

26. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the fast page mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

27. The system of claim 26, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

28. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and fast page mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the fast page mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller;

wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

29. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and extended data out mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of

access control signal timing requirements for the extended data out mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

30. The system of claim 29, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

31. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device which is interchangeably of a mode selected from the group consisting of burst extended data out mode and extended data out mode, the memory having a first set of access control signal timing requirements for the burst extended data out mode and a second set of access control signal timing requirements for the extended data out mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller;

wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

32. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signals and the second set of access control signals to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

33. The system of claim 32, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

34. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signals and the second set of access control signals to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller;

wherein the processor is responsive to at least information from the memory to program the memory controller to provide the first set of access control signals to the memory at a first time and the second set of access control signals to the memory at a second time.

35. A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank.

36. The system of claim 35, wherein the memory type of the second bank is interchangeable.

37. A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory.

38. A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank, the access control signals being driven in the first and second modes in response to information obtained by reading the first and second banks, respectively.

39. A system, comprising:

a memory controller; and

a memory, wherein the memory comprises:

a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory, and controls access of the first bank in accordance with one of the first and second sets of requirements based on information obtained by reading the first bank, and controls access of the second bank

in accordance with one of the first and second sets of requirements based on information obtained by reading the second bank.

40. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory; and

a processor, coupled to the bus and the memory controller, responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

41. The system of claim 40, further comprising:

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller in accordance with the memory device mode.

42. A system, comprising:

a bus for transferring information;

a memory, coupled to the bus, comprised of a memory device operable in a mode selected from the group consisting of burst extended data out mode and a second operation mode, wherein the memory has a first set of access control signals for operation in the burst extended data out mode and a second set of access control signals for operation in the second operation mode;

a programmable memory controller, coupled to the bus and to the memory, capable of providing the first set of access control signal timing requirements and the second set of access control signal timing requirements to the memory;

a processor, coupled to the bus and the memory controller;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the memory device mode and to program the memory controller, wherein the processor is responsive to at least information from the memory to program the memory controller to provide a set of access control signals to the memory in accordance with the memory device mode, wherein the information from the memory includes data read from the memory device.

43. A system, comprising:

a processor;

a memory controller coupled to the processor; and

a memory coupled to the memory controller, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of

extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second modes.

44. The system of claim 43, wherein the power up detection circuit is responsive to a signal from the power supply to program the memory controller in accordance with the first and second modes.

45. A system, comprising:

a processor;

a memory controller coupled to the processor; and

a memory coupled to the memory controller, wherein the memory includes a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power

up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements.

46. The system of claim 45, wherein the power up detection circuit is responsive to a signal from the power supply to program the memory controller in accordance with the first and second sets of requirements.

47. A system, comprising:

a processor;

a memory controller coupled to the processor; and

a memory coupled to the memory controller, wherein the memory comprises:

a first bank of burst extended data out memory coupled to the memory controller to receive a plurality of access control signals; and

a second bank comprised of a memory type selected from the group consisting of extended data out memory and fast page mode memory, wherein the second bank is coupled to the memory controller to receive the plurality of access control signals, further wherein the memory controller drives the access control signals in a first mode to provide access to the first bank, still further wherein the memory controller drives the access control signals in a second mode to provide access to the second bank, the access control signals being driven in the first and second modes in response to information obtained by reading the first and second banks, respectively;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second modes.

48. The system of claim 47, wherein the power up detection circuit is responsive to a signal from the power supply to program the memory controller in accordance with the first and second modes.

49. A system, comprising:

a processor;

a memory controller coupled to the processor; and

a memory coupled to the memory controller, wherein the memory includes a first bank and a second bank, wherein the first bank and the second bank are each independently interchangeably of a memory type selected from the group consisting of burst extended data out memory and a second type of memory, further wherein the memory controller controls access of the first bank and second bank in accordance with a first set of requirements for the burst extended data out memory and a second set of requirements for the second type of memory, and controls access of the first bank in accordance with one of the first and second sets of requirements based on information obtained by reading the first bank, and controls access of the second bank in accordance with one of the first and second sets of requirements based on information obtained by reading the second bank;

a power supply; and

a power up detection circuit coupled to the processor and to the power supply, the power up detection circuit responsive to a signal from the power supply to cause the processor to detect the first and second sets of requirements and to program the memory controller in accordance with the first and second sets of requirements.

S/N 09/510,375 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Brett L. Williams	Examiner: Hong Kim
Serial No.:	09/510,375	Group Art Unit: 2185
Filed:	February 22, 2000	Docket: 303.164US3
Title:	SYSTEM SUPPORTING MULTIPLE MEMORY MODES INCLUDING A BURST EXTENDED DATA OUT MODE	

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant further request that a copy of the 1449 form, initialled by the Examiner to indicate that all listed citations have been considered, be returned with the next official communication.

Applicant have included the fee of $180.00 under 37 C.F.R. §§ 1.97(c) and 1.17(p). Please charge any additional fees or credit any overpayment to Account No. 19-0743.

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

BRETT L. WILLIAMS

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6913

Date 9/19/2001 By _____
Edward J. Brooks, III
Reg. No. 40,925

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 19th day of September, 2001.

Amy Moriarty
Name

Amy Moriarty
Signature

Form 1449*	Atty. Docket No.: 303.164US3	Serial No. 09/510,375
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)	Applicant: Brett L. Williams	
	Filing Date: February 22, 2000	Group: 2185

U.S. PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS

**Examiner Initial	Document Number	Date	Country	Class	Subclass	Translation Yes	Translation No

OTHER DOCUMENTS
(Including Author, Title, Date, Pertinent Pages, Etc.)

**Examiner Initial	
	"16MS DRAM Schematics", Micron Technology, pp. 1-58, (February 1993)
	"2Mx8 Synchronous DRAM Schematics, Rev. 1.9", Micron Technology, pp. 357495-357595, (December 1995)
	"2Mx8 Synchronous Dram Schematicsm, Rev. 1.5", Micron Technology, pp. 1-85, (May 1994)
	McAlexander, J.C., Third Supplemental Expert Report, In the U.S District Court for the District of Delaware; Mosel Vitelic Coporation, Plaintiff, v. Micron Technology, Inc., Defendant; Micron Technology Inc., Counter-Plaintiff, v. Mosel Vitelic Corporation and Counter-Defendants; No. 98-449-GMS, pp. 1-28, (1998)

Examiner	Date Considered

*Substitute Disclosure Statement Form (PTO-1449)

**EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.